MS 43 (NS)

IV Semester M.Sc. (I.T.) Examination, June/July 2010
VLSI

Time : 3 Hours Max. Marks : 75

Instruction *: Answer* ***all*** *questions from Part* ***A****, and answer* ***any five*** *question from Part* ***B****.*

PART – A

1. What is absolute value ? **(12×2+1×1=25)**
2. What is underflow ?
3. Write the applications of DSP.
4. Write the features of multiplier.
5. Write the functioning difference between ALU and shifter.
6. Write the characteristics of MIMD.
7. List VLSI design styles.
8. Write the layout design rules.
9. Define CMOS n wells process.
10. What is interconnect resistance estimation.
11. How does MAC work ?
12. Write the steps in fabrication process flow.
13. Define carry save.

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PART – B

Answer **any five** : **(5×10=50)**

1. Explain divide and conquer technique estimation involved in VLSI systems.
2. Discuss standard cell based design and full systems design.
3. Explain different types of advanced CMOS fabrication techniques.
4. What is complex CMOS logic gates ? Explain in detail.
5. Write brief notes on
   a) Time division multiple access.
   b) Frequency division multiple access.
   c) Code Division Multiple access.
6. Explain media sharing and node sharing technique.
7. What is super scalar architecture ? Explain different types.
8. Briefly explain
   a) Switching power dissipation.
   b) Short circuit power dissipation.

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